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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/121,175	07/22/1998	RICHARD B. MERRILL	FOV-011	3033

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EXAMINER	
YE, LIN	
ART UNIT	**PAPER NUMBER**
2612	

DATE MAILED: 07/25/2002

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/121,175	MERRILL ET AL.
	Examiner	Art Unit
	Lin Ye	2612

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 May 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,21-36 and 48-57* is/are pending in the application.

4a) Of the above claim(s) *10-20,37-47,58 and 59* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,21-36 and 48-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4,6,7,13* . 15/16
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Species of Figure 5 which read on claims 1-9, 21-36 and 48-57 in Paper No. 18 filed on May 13, 2002 is acknowledged.
2. Claims 10-20, 37-47,58 and 59 withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Species, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 18 filed on May 13, 2002.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1-9, 21-36, and 48-57 are rejected under 35 U.S.C. 102(e) as being anticipated by Merrill et al. U.S. Patent 5,962,844 (Hereinafter referred to as Merrill).

Referring to claim 1, Merrill reference discloses in Figures 8A, 4 and 3, an active pixel sensor (pixel cell 400, Col.8, line 52) disposed on a semiconductor substrate, comprising a photosensor (sensor 402, Col. 8, line 58) having a first terminal and a second terminal, said first terminal coupled to a first reference potential; a reset transistor (transistor 404, Col. 8, line 60) having a first terminal coupled to said second terminal of said photosensor, a second terminal coupled to a reset potential, and a third terminal coupled to a reset line (row reset line124, Col. 7, line 31); and a plurality of storage nodes (node 1 &2 with storage elements 410 & 412) coupled to said second terminal of said photsensor (402) (See Col. 8, lines 58-62).

Referring to claim 2, an active pixel sensor (400) further including means coupled to plurality of storage nodes (node 1 &2 with storage elements 410 & 412) for outputting a value from any of said plurality of storage nodes (See. Col. 9, lines 5-7).

Referring to claim 3 An active pixel sensor (400) includes a plurality of transfer lines (x & xbr), wherein each separate on of said plurality of storage nodes is coupled to said second terminal of said photsensor by a separate on of a plurality of transfer transistors having a first terminal connected to said second terminal of said photsensor (in contrast with the pixel design of figures 3 and 4, transfer transistors n2 & n4 connected to second terminal of photosensor 120), a second terminal connected to said separate one of said plurality of storage nodes, and a third terminal connected to separate one of said plurality of transfer lines.

Referring to claim 4, an active pixel sensor (400) includes each separate one of said plurality of storage nodes is coupled to said means for outputting a value from any of said plurality of storage nodes by a separate one of a plurality of readout transistors (414 & 416, Col. 8, line 66) having a first terminal connected to said separate one of said plurality of storage nodes, a second terminal coupled to a second potential, and a third terminal connected to said means for outputting a value from any of said plurality of storage nodes (See Col. 8, lines 66-67).

Referring to claim 5, an active pixel sensor (400) further including a plurality of storage elements (410 & 412, shown as capacitors) each separate one of said storage elements having a first terminal coupled to a separate one of said storage nodes, and a second terminal coupled to a second reference potential.

Referring to claim 6, an active pixel sensor (100) means for outputting a value includes: a plurality of column output lines (202 & 204); a row select line (128); and a plurality of row select transistors (n3 and n5), each of said row select transistors having a first terminal coupled to one of said plurality of storage nodes, a second terminal coupled to one of said plurality of column output lines, and a third terminal coupled to said row select line.

Referring to claim 7, an active pixel sensor (400) including plurality of transfer lines (x & xbar), wherein each separate one of plurality of storage nodes is coupled to said second terminal of said photosensor (402) by a separate one of a plurality of transfer transistors (406 & 408) having a first terminal connected to said second terminal of said photosensor (402), a second terminal connected to said separate one of said plurality of storage nodes, and a third terminal connected to a separate one of said plurality of transfer lines (x & xbar).

Referring to claim 8, an active pixel sensor (400) has wherein each separate one of said plurality of storage nodes (node 1 &2 with storage elements 410 & 412) is coupled to said first terminal of a separate one of said plurality of row select transistors (418) by a separate one of a plurality of readout transistors having a first terminal connected to said separate one of said plurality of storage nodes, a second terminal coupled to a second potential, and a third terminal coupled to said first terminal of said separate one of said plurality of row select transistors.

Referring to claim 9 an active pixel sensor (400) includes a plurality of storage elements (node 1 &2 with storage elements 410 & 412), each separate one of said storage elements having a first terminal coupled to a separate one of said storage nodes, and a second terminal coupled to a second reference potential.

Referring to claim 21 an active pixel sensor (100 0r 400) means for outputting a value includes: a plurality of column output lines; a plurality of row select lines as shown in figure 4; and a plurality of row select transistors (n3 & n5), each of said row select transistors having a first terminal coupled to one of said plurality of storage nodded, a second terminal coupled to on e of said plurality of column output lines, and a third terminal coupled to one of said plurality of row select lines.

Referring to claim 22, an active pixel sensor (100 or 400), further including a plurality of transfer lines, wherein each separate one of said plurality of storage nodes is coupled to said second terminal of said photosensor by a separate one of a plurality of transfer transistors having a first terminal connected to said second terminal of said photosensor, a second

terminal connected to said separate one of said plurality of storage nodes, and a third terminal connected to a separate one of said plurality of transfer lines.

Referring to claim 23, an active pixel sensor (100 or 400) wherein each separate one of said plurality of storage nodes is coupled to said first terminal of one of said plurality of row select transistors by a separate one of a plurality of readout transistors having a first terminal connected to said one of said plurality of storage nodes, a second terminal coupled to a second potential, and a third terminal coupled to said first terminal of said one of said plurality of row select transistors as shown in figure 4.

Referring to claim 24 An active pixel sensor (100 0r 400), further including a plurality of storage elements, each separate one of said storage elements having a first terminal coupled to a separate one of said storage nodes, and a second terminal coupled to a second reference potential.

Referring to claim 25, an active pixel sensor (100 or 400), wherein said means for outputting a value includes: a row select line (128); a column bias line; first and second column output lines; a row select transistor having a first terminal coupled to said row select line, second terminal coupled to said column bias line, and a third terminal; and wherein said plurality of storage nodes includes a first node and second storage node, said first storage node is coupled to said means for outputting a value by a first readout transistors having a first terminal coupled to said first storage node, a second terminal coupled to said first column output line, and a third terminal connected to said third terminal of said row select transistor (418 or n3 and n5), and said second storage node is coupled to said means for outputting a value by a second readout transistor having a first terminal coupled to said

second storage node, a second terminal coupled to said second column output line, and a third terminal connected to said third terminal of said row select transistor (418 or n3 and n5).

Referring to claim 26, an active pixel sensor (100 or 400), further including a plurality of transfer lines (x & xbar), wherein each separate one of said plurality of storage nodes is coupled to said second terminal of said photosensor by a separate one of a plurality of transfer transistors having a first terminal connected to said second terminal of said photosensor, a second terminal connected to said separate one of said plurality of storage nodes, and a third terminal connected to a separate one of said plurality of transfer lines.

Referring to claim 27, an active pixel sensor (400), further including a plurality of storage elements (410 & 412), each separate one of said storage elements having a first terminal coupled to a separate one of said storage nodes, and a second terminal coupled to a second reference potential.

Referring to claim 28. An active pixel sensor disposed on a semiconductor substrate, comprising: comprising a photosensor (402) having a first terminal and a second terminal, said first terminal coupled to a first reference potential; a reset transistor (404) having a first terminal coupled to said second terminal of said photosensor, a second terminal coupled to a reset potential, and a third terminal coupled to a reset line (124); and a plurality of storage nodes (node 1 &2 with storage elements 410 & 412) coupled to a separate one of said second terminal of said photsensor (402) (See Col. 8, lines 58-62).

Referring to claim 29 is considered substantively equivalent to claim 2 discussed above.

Referring to claim 30 is considered substantively equivalent to claim 3 discussed above.

Referring to claim 31 is considered substantively equivalent to claim 4 discussed above.

Referring to claim 32 is considered substantively equivalent to claim 5 discussed above.

Referring to claim 33 is considered substantively equivalent to claim 6 discussed above.

Referring to claim 34 is considered substantively equivalent to claim 7 discussed above.

Referring to claim 35 is considered substantively equivalent to claim 8 discussed above.

Referring to claim 36 is considered substantively equivalent to claim 9 discussed above.

Referring to claim 48 is considered substantively equivalent to claim 21 discussed above.

Referring to claim 49 is considered substantively equivalent to claim 22 discussed above.

Referring to claim 50 is considered substantively equivalent to claim 23 discussed above.

Referring to claim 51 is considered substantively equivalent to claim 24 discussed above.

Referring to claim 52 is considered substantively equivalent to claim 25 discussed above.

Referring to claim 53 is considered substantively equivalent to claim 26 discussed above.

Referring to claim 54 is considered substantively equivalent to claim 27 discussed above.

Referring to claim 55,a method of operating an active pixel sensor having a photosensor (402), a reset transistor (404), a plurality of storage nodes (node 1 & 2) coupled to said photosensor and means coupled to said plurality of storage nodes for outputting a value from any of said plurality of storage nodes comprising the steps of: turning on the reset transistor to place a reset potential on said photosensor; transferring charge from said photosensor to a first of the plurality of storage nodes for a first duration; and transferring charge from said photosensor to a second of the plurality of storage nodes for a second duration (See Col. 9, lines 5-13).

Referring to claim 56, a method of operating an active pixel sensor (400) includes wherein said first duration commences coincident with said second duration (See Col. 9, lines 20-29, the new integrated output starts end of the current integration interval).

Referring to claim 57, a method of operating an active pixel sensor (400) includes wherein said second duration commences after said first duration has ended (See Col. 9, lines 30-35).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

   a. Beiley, US. Patent 6,243134 reference discloses in figure 5, two storage elements (C2 & C3) with separate storage nodes (D & E).

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Lin Ye** whose telephone number is **(703) 305-3250**. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy R Garber can be reached on (703) 305-4929.

   Any response to this action should be mailed to:

   Commissioner of Patents and Trademarks

   Washington, DC. 20231

   Or faxed to:

(703) 872-9314

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal drive, Arlington, VA., Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Lin Ye
July 24, 2002

TUAN HO
PRIMARY EXAMINER